## REMARKS

Claims 1-12, 14-16 and 18-20 are pending in the present application. Claims 1-12, 14-16 and 18-20 are rejected. Claims 1 and 3 have been amended, and claims 1-4 are independent. Reconsideration in view of the following arguments is kindly requested.

## Examiner Interview

Applicant thanks the Examiner for the courtesies extended during the telephonic interview conducted on December 6, 2004. During the interview, Applicant discussed the 35 U.S.C. § 102(b) rejection to claim 1. With regard to claim 1, Applicants argued that Fig. 1 and column 1 of Surlekar do not disclose all of the features recited in claim 1, specifically, a data output buffer for transferring the internal signals externally. The Examiner disagreed and asserted that Fig. 1 of Surlekar illustrated internal signals (e.g. RAS_, CAS_, W_ and G_ input from timing and control unit 19) being transferred externally via the data out register 17. Applicants disagree that the mere coupling of circuit components (i.e. timing and control unit 19, input/output buffer 16 and data out register 17) constitutes transferring internal signals externally. Therefore, Applicant and the Examiner did not reach an agreement regarding the discussion of claim 1.

The above discussion, which is believed to satisfy the requirements of MPEP 713.04, is intended as an explanation only and is not intended to limit the invention defined by the claims of the present application.

The remainder of this Amendment further summarizes and supplements the patentability arguments that were presented during the interview.

## Claim Rejections – 35 U.S.C. § 102

Claims 1-12, 14-16 and 18-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Surlekar, USP 5,668,764. This rejection is respectfully traversed.

Applicant submits that the Examiner has relied on a broad portion of Surlekar with a lack of specificity with regard to the rejection of claim 1.

In the advisory action dated December 1, 2004, the Examiner alleges:

> "Surlekar teaches in Figure 1 in conjunction with col. 1, lines 14-65, in part, "output signals from the timing and control unit 19 are applied to the data input/output buffers 16" which are external".

Applicants submit that the above noted portions of Surlekar (col. 1, lines 14-65 and Figure 1) do not explicitly teach the output signals of the timing and control unit 19 (i.e., internal signals) being transferred externally.

Applicants have amended claim 1 to better clarify the operation of transferring the internal signals externally. Claim 1 as amended recites, transferring the internal signals externally from the integrated circuit device through data input/output pads in response to an output enable signal. Nowhere does Surlekar teach or disclose transferring the internal signals externally... in response to an output enable signal, as recited in claim 1.

Surlekar discloses data input/output buffer 16 configured to output data signals externally, which are input from memory array unit 15. See column 1, lines 35-42 of Surlekar. The data input/output buffer 16 receives internal data signals (i.e. control signals and address signals), and data from memory array 15 and register 18. However, nowhere does the specification of Surlekar recite transferring the internal signals externally from the integrated circuit device through data input/output pads in response to an output enable signal, as recited in claim 1.

Accordingly, Applicant submits that claim 1 and those claims dependent thereon are allowable over the prior art. Withdrawal of this rejection is kindly requested.

Regarding claim 2, Applicants submit that Surlekar fails to teach or disclose all of the features recite in claim 2. For example, nowhere does Surlekar disclose a second selection circuit for receiving output signals from the first selection circuit and output signals from a sense amplifier, and for opening an alternative one of transfer paths for the internal signals and the output signals of the sense amplifier in response to the selection signals, as recited in claim 2.

Accordingly, Applicant submits that claim 2 and those claims dependent thereon are allowable over the prior art. Withdrawal of this rejection is kindly requested.

Regarding claim 3, Applicants submit that Surlekar fails to teach or disclose all of the features recited in claim 3. For example, nowhere does Surlekar disclose selecting a part of internal signals of the integrated circuit device in response to selection signals, the internal signals used for addressing storage locations and for controlling internal operations.

Accordingly, Applicant submits that claim 3 and those claims dependent thereon are allowable over the prior art. Withdrawal of this rejection is kindly requested.

Regarding claim 4, for similar reasons as those stated above with regard to claim 3, Applicants submit that claim 4 and those claims dependent thereon are also allowable over the prior art. Withdrawal of the rejection to these claims is also kindly requested.

## CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-12, 14-16 and 18-20 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____
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